IN THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method comprising:

evaluating one or more source characters to determine an intermediate running disparity for each of the one or more source characters; and

determining a running disparity for each of the one or more source characters before encoding the one or more source characters based on a current running disparity associated with the one or more source characters and the intermediate running disparity of each of the one or more source characters.

2. (Previously presented) The method of claim 1, wherein evaluating the one or more source characters comprises evaluating each of the one or more source characters to determine a flip/hold bit based on whether a respective source character will invert or maintain the current running disparity.

3. (Previously presented) The method of claim 2, wherein determining the running disparity for each of the one or more source characters comprises

comparing the flip/hold bit of the respective source character with the current running disparity.

4. (Previously presented) The method of claim 3, wherein determining the running disparity for each character comprises using an exclusive or (XOR) function to compare the flip/hold bit with the current running disparity.

5. (Canceled).

6. (Previously presented) The method of claim 1, wherein evaluating the one or more source characters comprises using one or more logic gates to determine whether each of the one or more source characters will invert or maintain the current running disparity.

7. (Previously presented) The method of claim 1, further comprising passing the current running disparity, the running disparity of each of the one or more source characters, and the one or more source characters to an encoder to encode the one or more source characters into one or more transmission characters.

8. (Currently amended) A circuit comprising:

a decoder to determine a flip/hold bit for each of a plurality of source characters based on whether a respective source character will invert or maintain a current running disparity associated with the plurality of source characters;

a pre-calculator to determine an intermediate running disparity for each of the plurality of source characters; and

a comparator coupled to the decoder and the pre-calculator to compare the ~~flip/hold bit~~ intermediate running disparity of each of the plurality of source characters with the current running disparity to determine a running disparity for the respective source character before the respective source character is encoded.

9. (Original) The circuit of claim 8, wherein the comparator comprises one or more exclusive or (XOR) gates.

10. (Canceled).

11. (Currently amended) The circuit of claim [[10]] 8, wherein the pre-calculator comprises one or more exclusive or (XOR) gates.

12. (Previously presented) The circuit of claim 8, further comprising an encoder coupled to the comparator to receive the current running disparity, a plurality of

running disparities of the plurality of source characters, and the plurality of source characters and to encode the plurality of source characters to a plurality of transmission characters.

13. (Original) The circuit of claim 12, wherein the encoder is an 8B/10B encoder that does not contain disparity calculation circuitry.

14. (Previously presented) An apparatus comprising:

means for evaluating one or more source characters to determine an intermediate running disparity for each of the one or more source characters; and

means for determining a running disparity for each of the one or more source characters based on a current running disparity associated with the one or more source characters and the intermediate running disparity of each of the one or more source characters before the source character is encoded.

15. (Previously presented) The apparatus of claim 14, wherein the means for determining the running disparity for each of the one or more source characters comprises means for comparing a flip/hold bit with the current running disparity.

16. (Previously presented) The apparatus of claim 14, wherein the means for determining the running disparity for each of the one or more source characters comprises means for pre-calculating at least a portion of the running disparity.

17. (Canceled).

18. (Original) The apparatus of claim 14, wherein the means for evaluating the one or more source characters comprises one or more logic gates to determine whether each source character will invert or maintain the current running disparity.

19. (Previously presented) The apparatus of claim 14, further comprising an encoder coupled to the means for determining the running disparity for each of the one or more source characters to receive the current running disparity, the running disparity for each of the one or more source characters, and the one or more source characters and to encode the one or more source characters to one or more transmission characters.

20. (Original) The apparatus of claim 19, wherein the encoder is an 8B/10B encoder that does not contain disparity calculation circuitry.

21. (Previously presented) The method of claim 1, wherein evaluating the one or more source characters comprises using a lookup table to determine whether each of the one or more source characters will invert or maintain the current running disparity.